NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60512-01.TGZ
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER 370HR MUST CONFORM TO UL94V-0 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS AND ITS TOLERANCE SHALL BE VERIFIED AS PER THE DRILL CHART BEFORE PLATING.ALL VIA DIAMETERS AND ITS TOLERANCE SHALL BE VERIFIED AS PER THE DRILL CHART; ALL OTHER HOLE DIAMETERS SHELL BE VERIFIED AT AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

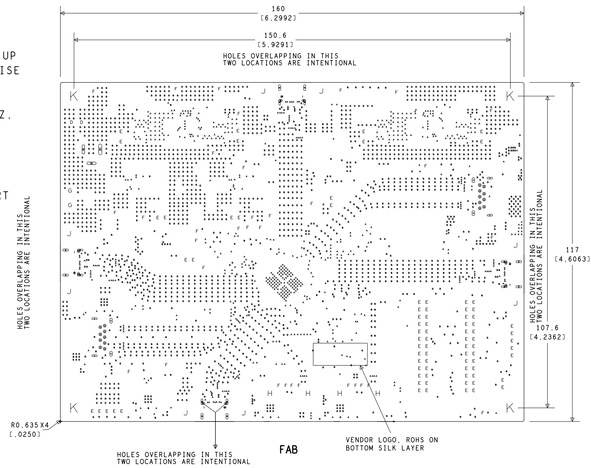
5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

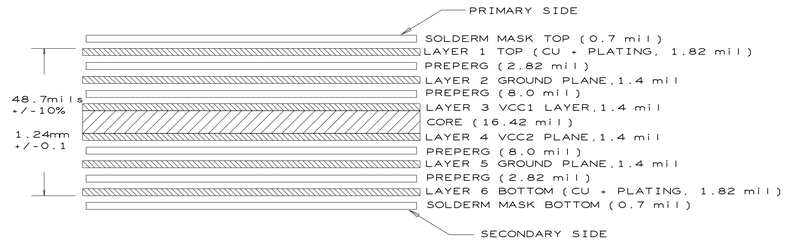
7. FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	0.2032	+0.0762/-0.0762	PLATED	713
·	0.254	+0.0762/-0.0762	PLATED	2451
⊕	0.7	+0.0762/-0.0762	PLATED	18
D	0.82	+0.0762/-0.0762	PLATED	2
E	1.016	+0.0762/-0.0762	PLATED	80
F	1.0201	+0.0762/-0.0762	PLATED	33
G	1.3	+0.0762/-0.0762	PLATED	2
H	2.3099	+0.0762/-0.0762	PLATED	4
·	0.6	+0.0508/-0.0508	NON-PLATED	4
J	2.2	+0.0508/-0.0508	NON-PLATED	8
K	3.1801	+0.0508/-0.0508	NON-PLATED	4
▬	1.2499x0.7	+0.0762/-0.0762	PLATED	4
▮	1.2499x0.7	+0.0762/-0.0762	PLATED	4
⊟	1.7x0.9	+0.0762/-0.0762	PLATED	4
∞	1.85x0.6	+0.0762/-0.0762	PLATED	4
∞	1.8999x0.5999	+0.0762/-0.0762	PLATED	4
∞	1.8999x0.5999	+0.0762/-0.0762	PLATED	4
∞	2.0x0.7	+0.0762/-0.0762	PLATED	4
∞	2.0x0.7	+0.0762/-0.0762	PLATED	4
⊡	3.175x0.889	+0.0762/-0.0762	PLATED	1
⊡⊡	3.175x0.889	+0.0762/-0.0762	PLATED	1
⊡	3.683x1.143	+0.0762/-0.0762	PLATED	1
•	0.8x0.6	+0.0508/-0.0508	NON-PLATED	2
•	0.8x0.6	+0.0508/-0.0508	NON-PLATED	2



NOTE: 4 MIL 5 MIL SPACING TRACES ON LAYER 1 DIFFERENTIAL IMPEDANCE CONTROLLED TO 90 OHMS +/- 10% TESTED

NOTE: 4 MIL 5 MIL SPACING TRACES ON LAYER 6 DIFFERENTIAL IMPEDANCE CONTROLLED TO 90 OHMS +/- 10% TESTED

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2

FINISH 7

THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES AUTHORIZATION FROM CYPRESS

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN HUSA	13/12/18
ENGINEER PRVE	13/12/18
CHECKER HITS	13/12/18
QA -	-
PROJ. ENG. -	-

CYPRESS EMBEDDED IN TOMORROW
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

TITLE: PCB FABRICATION,
CY6611 EZ-USB HX3PD EVK

SIZE	CAGE CODE	CY P/N
D	-	610-60512-01

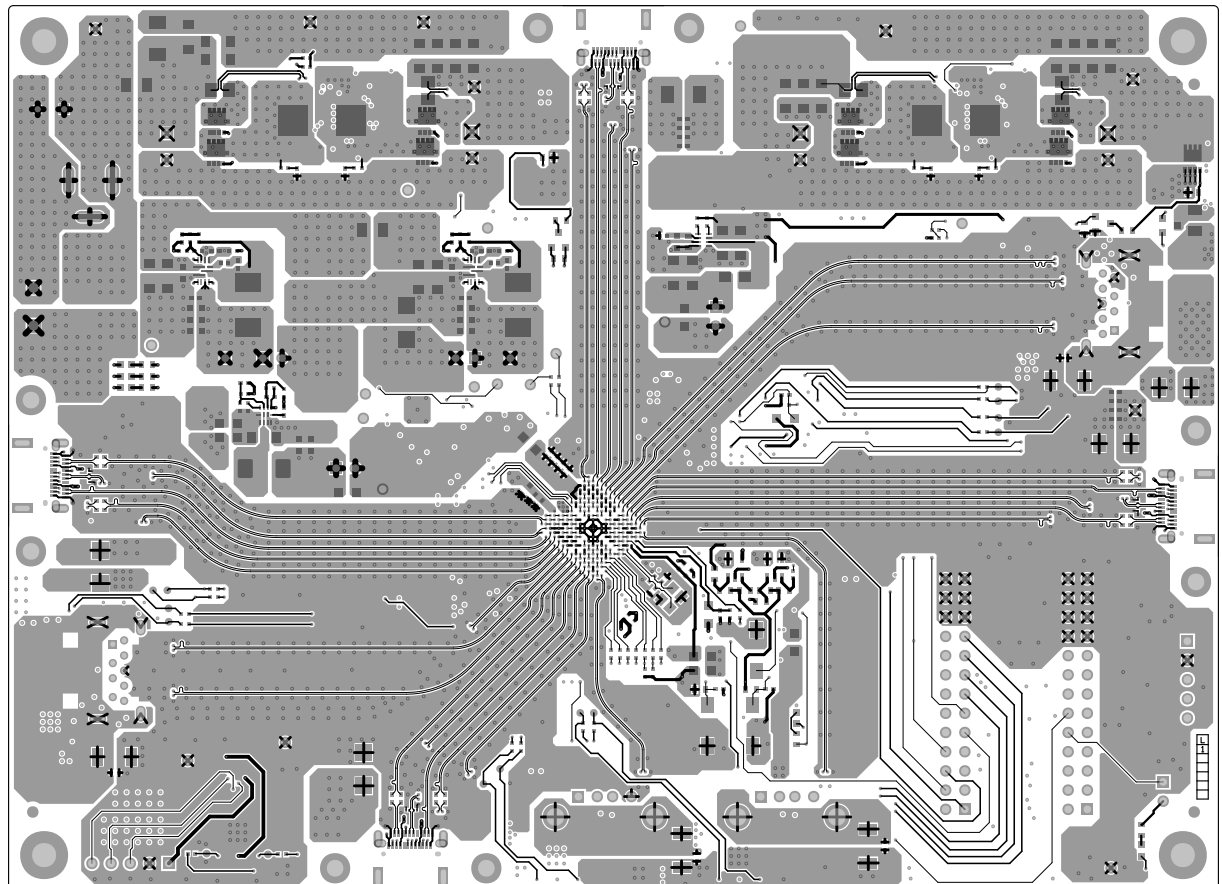
SCALE	SHEET	REV
1/1	1 OF 1	03

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-XXXXX-01_02.BRD

FAB NOTES REV 08/08/18

ART FILM - detail1



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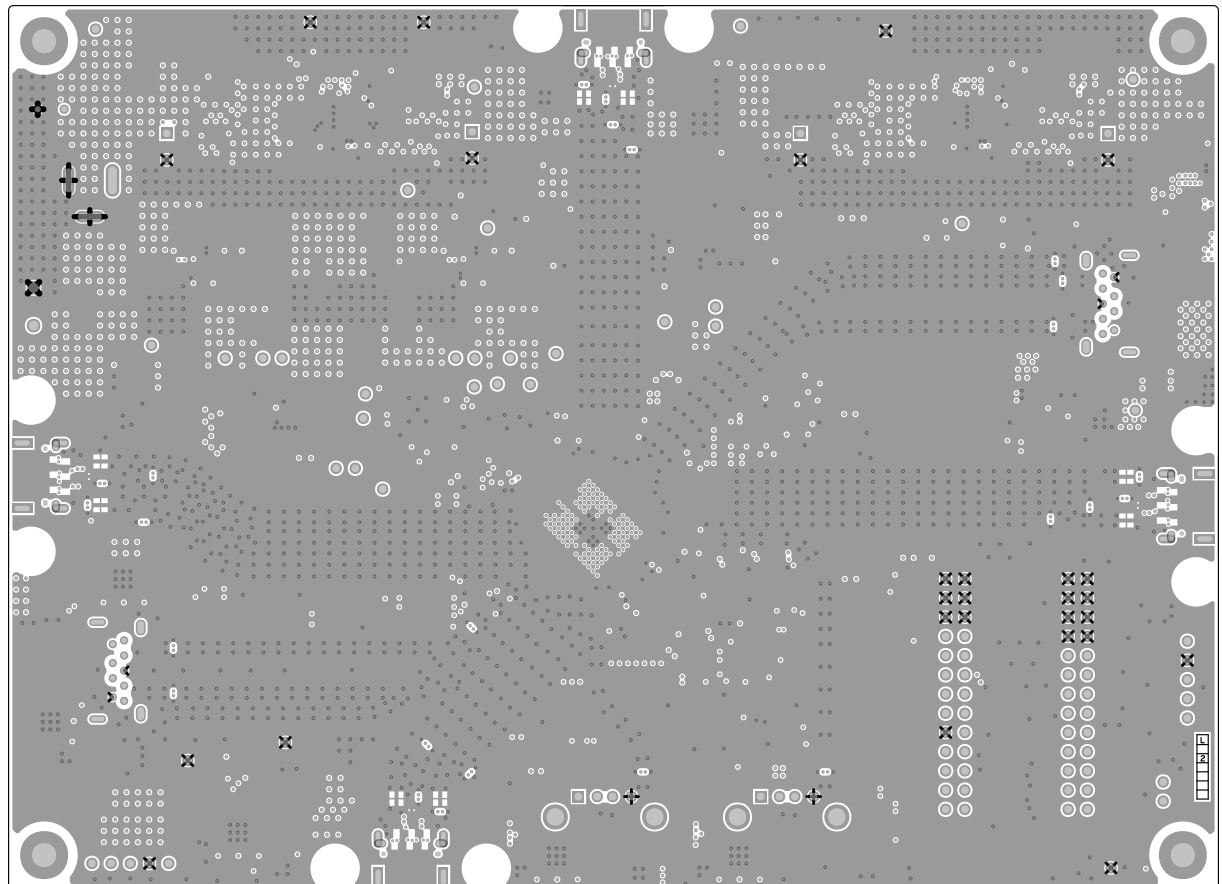
	LAYER: PRIMARY SIDE		
	DWG NO: 600-60512-01	REV: 03	DATE: 13/12/18



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	LAYER: GROUND1 LAYER		
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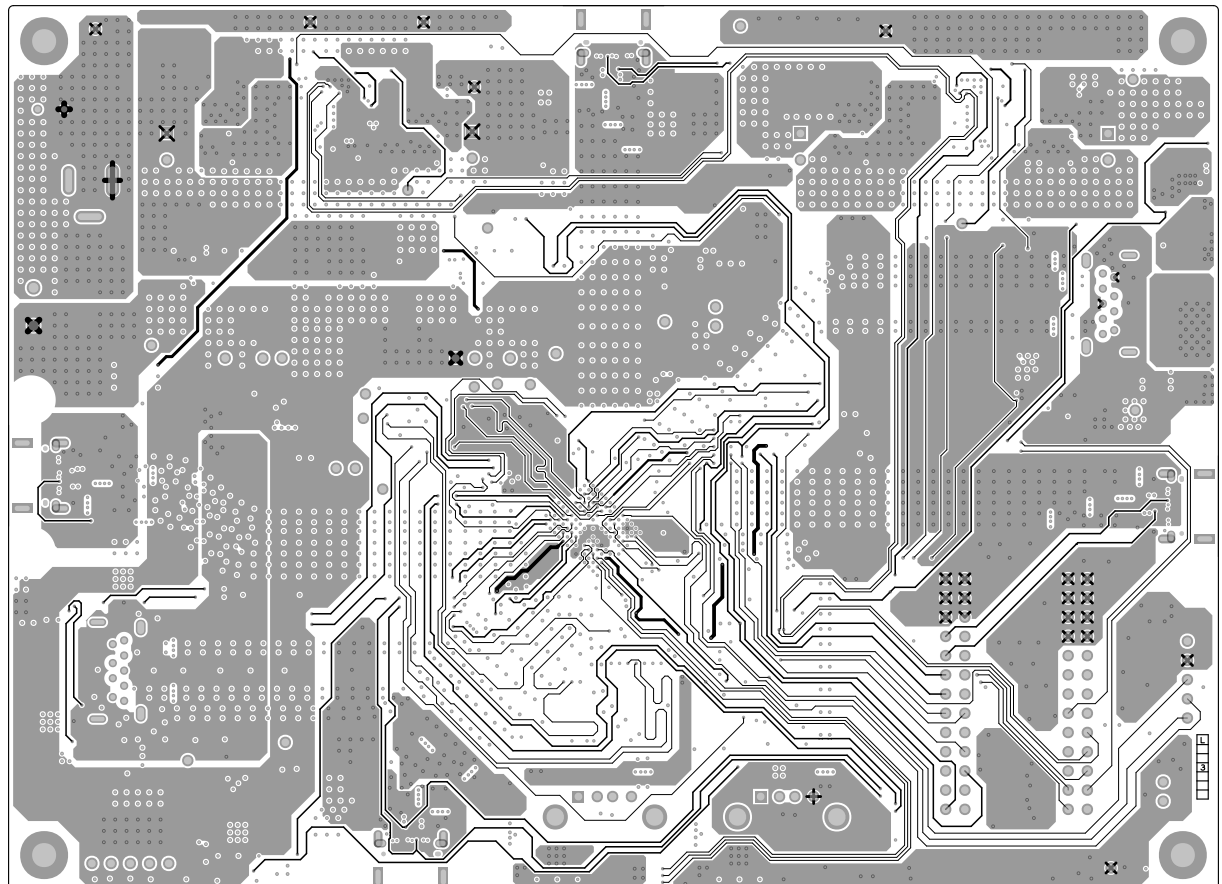

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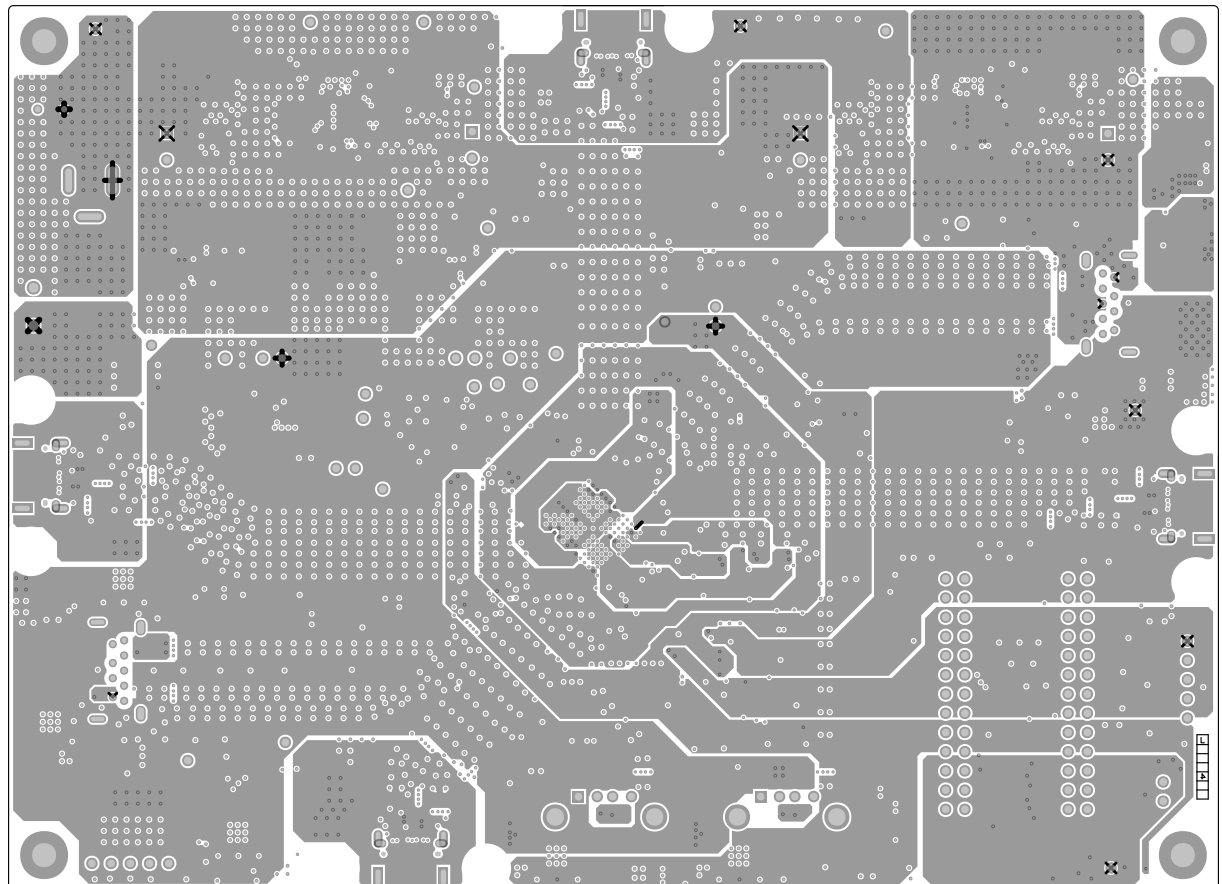

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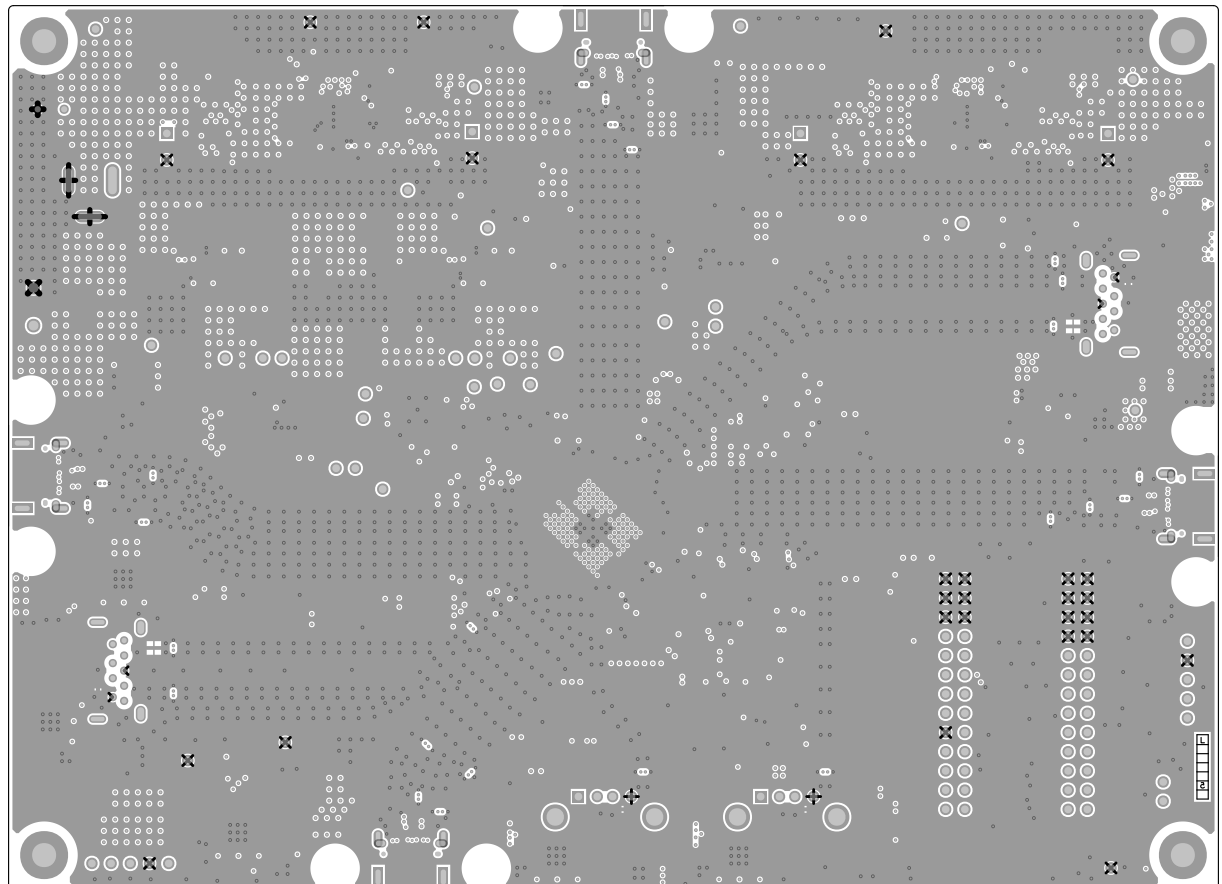
	DRAWN BY: HUSA		
	LAYER: POWER LAYER		
	DWG NO: 600-60512-01	REV: 03	DATE: 13/12/18



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	DRAWN BY: HUSA		
	LAYER: GROUND2 LAYER		
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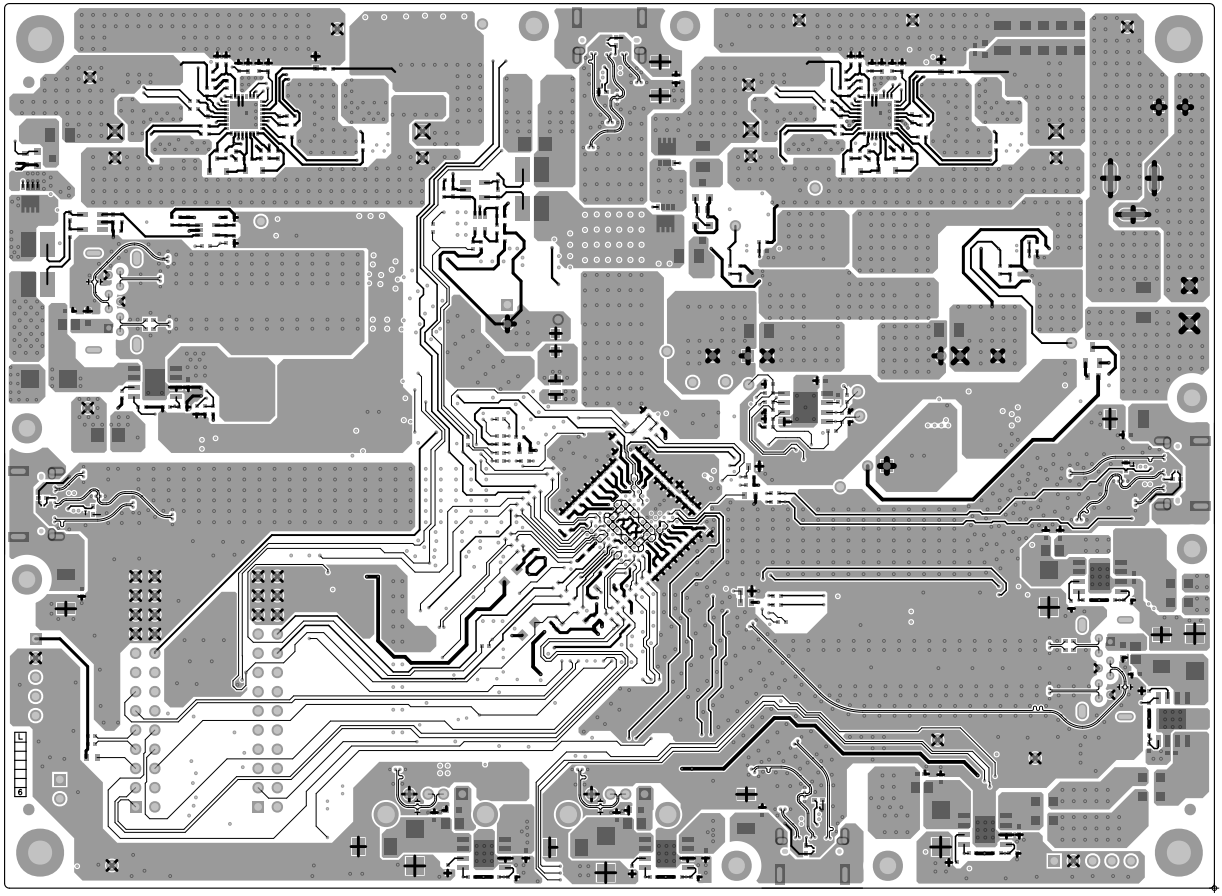

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	LAYER: SECONDARY SIDE		
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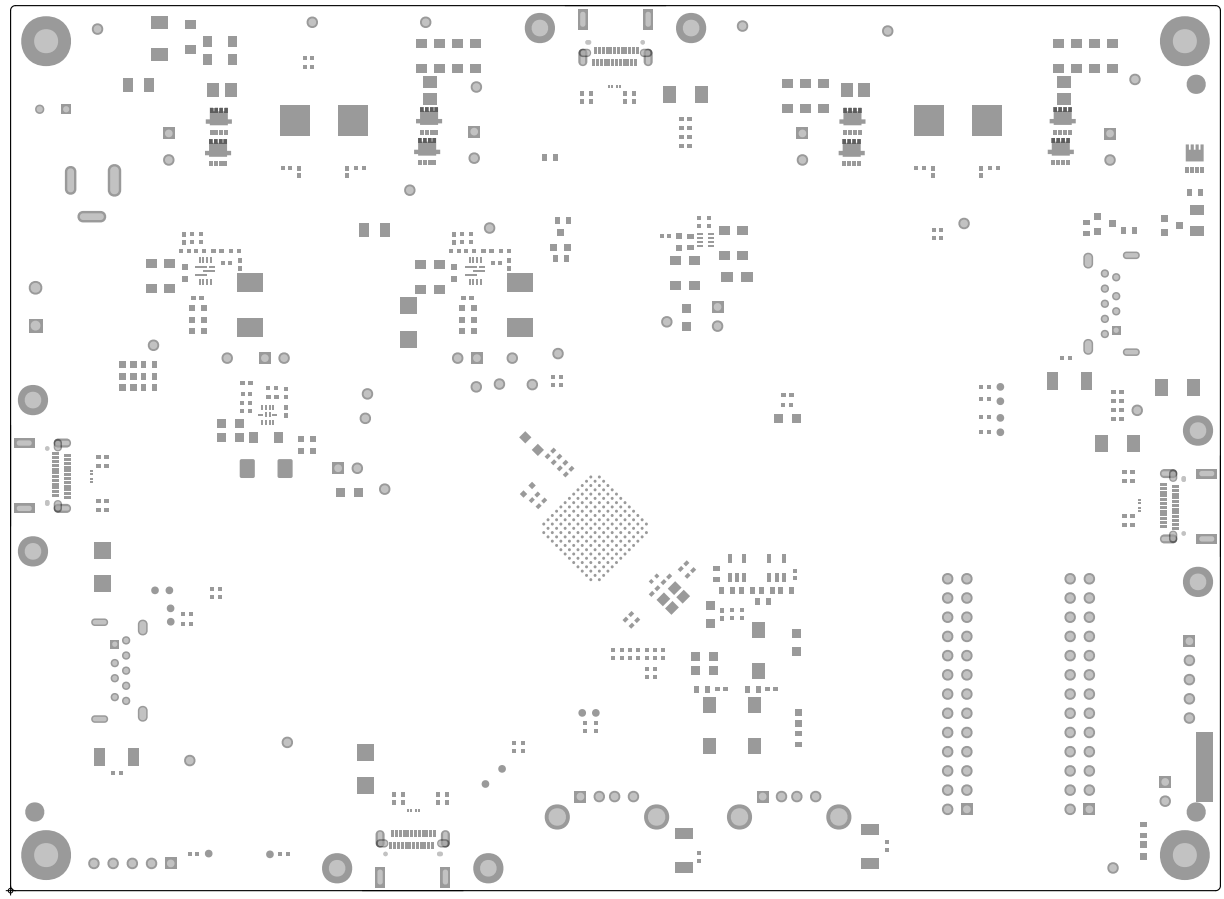

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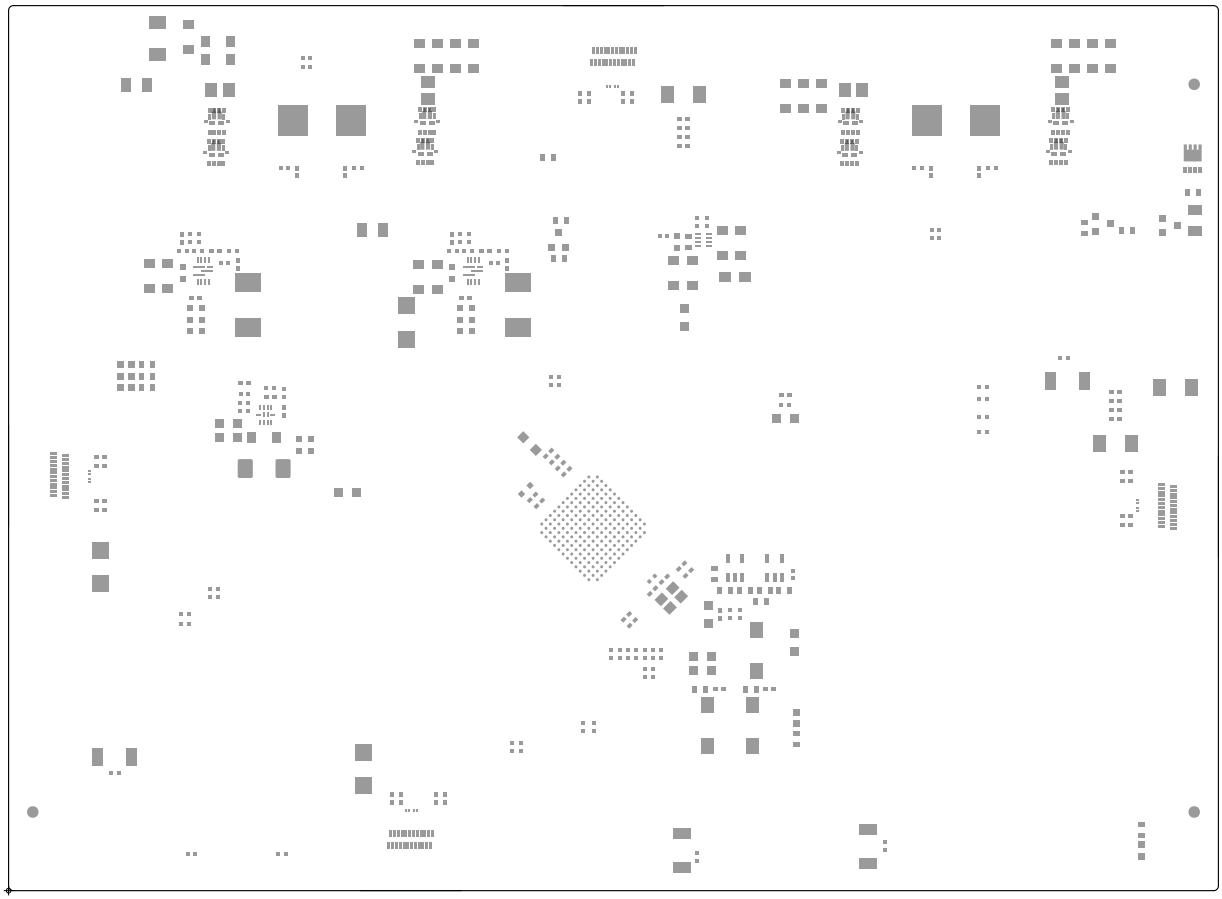
	DRAWN BY: HUSA		
	LAYER: PRIMARY SIDE SOLDERMASK		
SAN JOSE, CA 95134 (408) 943-2600	DWG NO: 600-60512-01	REV: 03	DATE: 13/12/18



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	LAYER: PRIMARY SIDE SOLDERPASTE		
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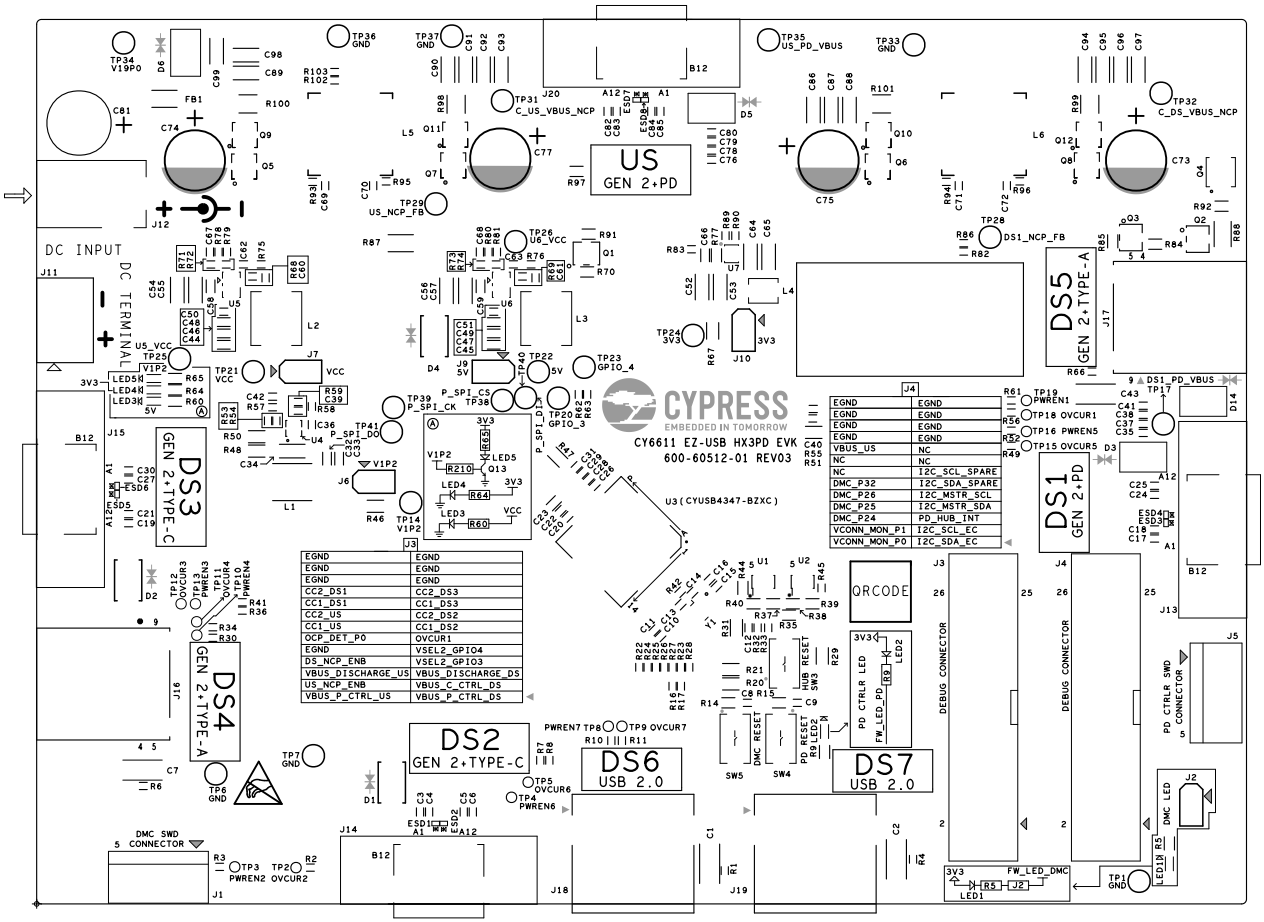
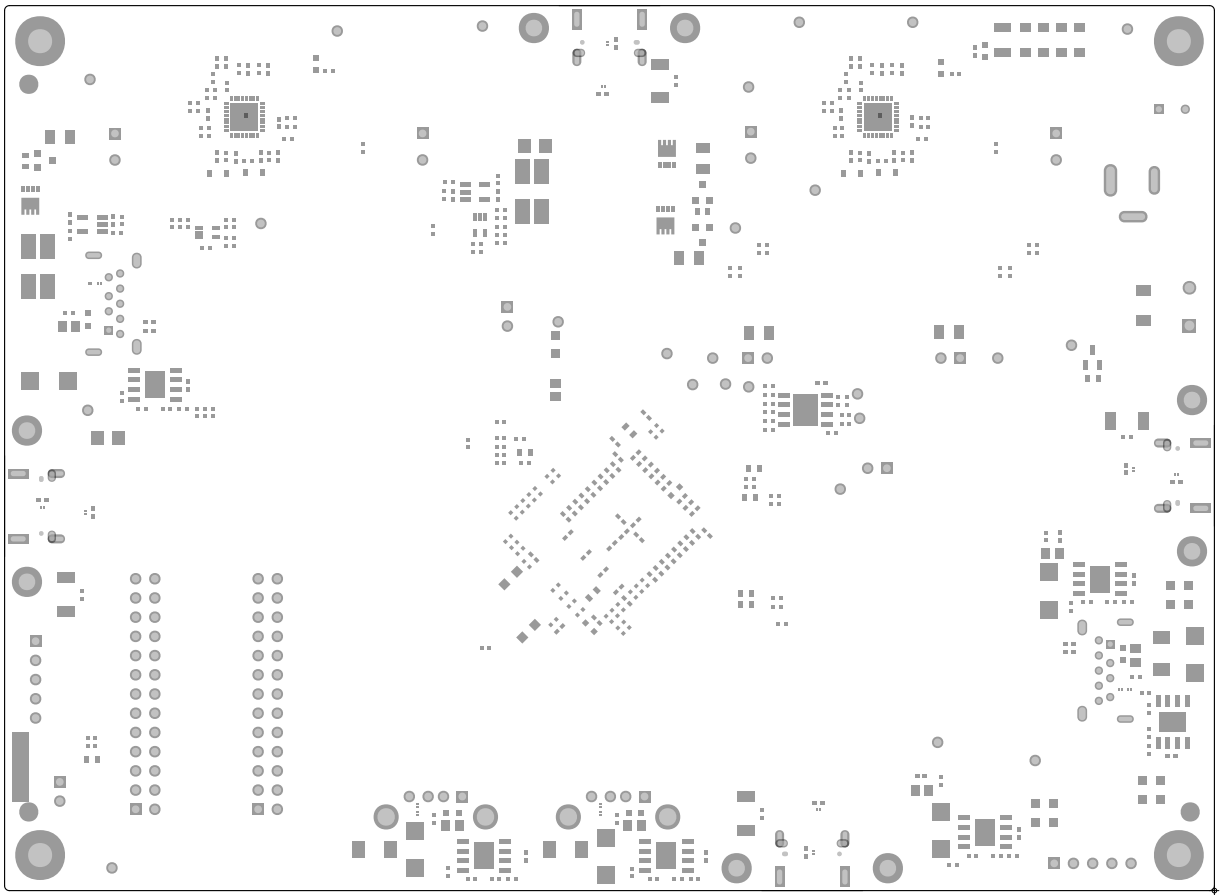


EGND	EGND
EGND	EGND
EGND	EGND
CC2_DS1	CC2_DS3
CC1_DS1	CC1_DS3
CC2_US	CC2_DS2
CC1_US	CC1_DS2
OCP_DET_P0	OVCUR1
EGND	VSEL2_GPIO4
DS_NCP_ENB	VSEL2_GPIO3
VBUS_DISCHARGE_US	VBUS_DISCHARGE_DS
US_NCP_ENB	VBUS_C_CTRL_DS
VBUS_P_CTRL_US	VBUS_P_CTRL_DS

EGND	EGND
EGND	EGND
EGND	EGND
EGND	EGND
VBUS_US	NC
NC	NC
NC	I2C_SCL_SPARE
DMC_P32	I2C_SDA_SPARE
DMC_P26	I2C_MSTR_SCL
DMC_P25	I2C_MSTR_SDA
DMC_P24	PD_HUB_INT
VCONN_MON_P1	I2C_SCL_EC
VCONN_MON_P0	I2C_SDA_EC

CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT:	BOARD NAME: CY6611 EZ-USB HX3PD EVK	
	DRAWN BY:	HUSA	
	LAYER:	PRIMARY SIDE SILKSCREEN	
	DWG NO: 600-60512-01	REV: 03	DATE: 13/12/18



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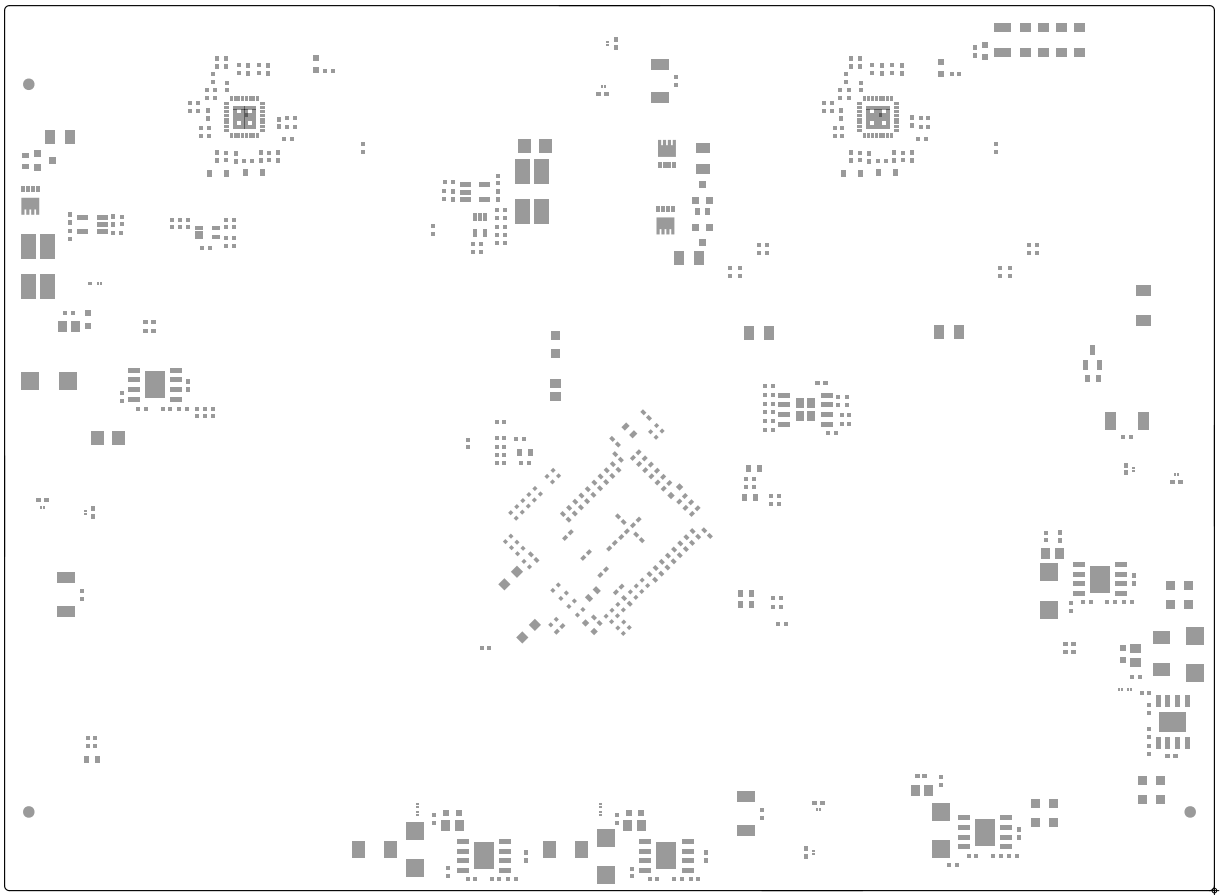

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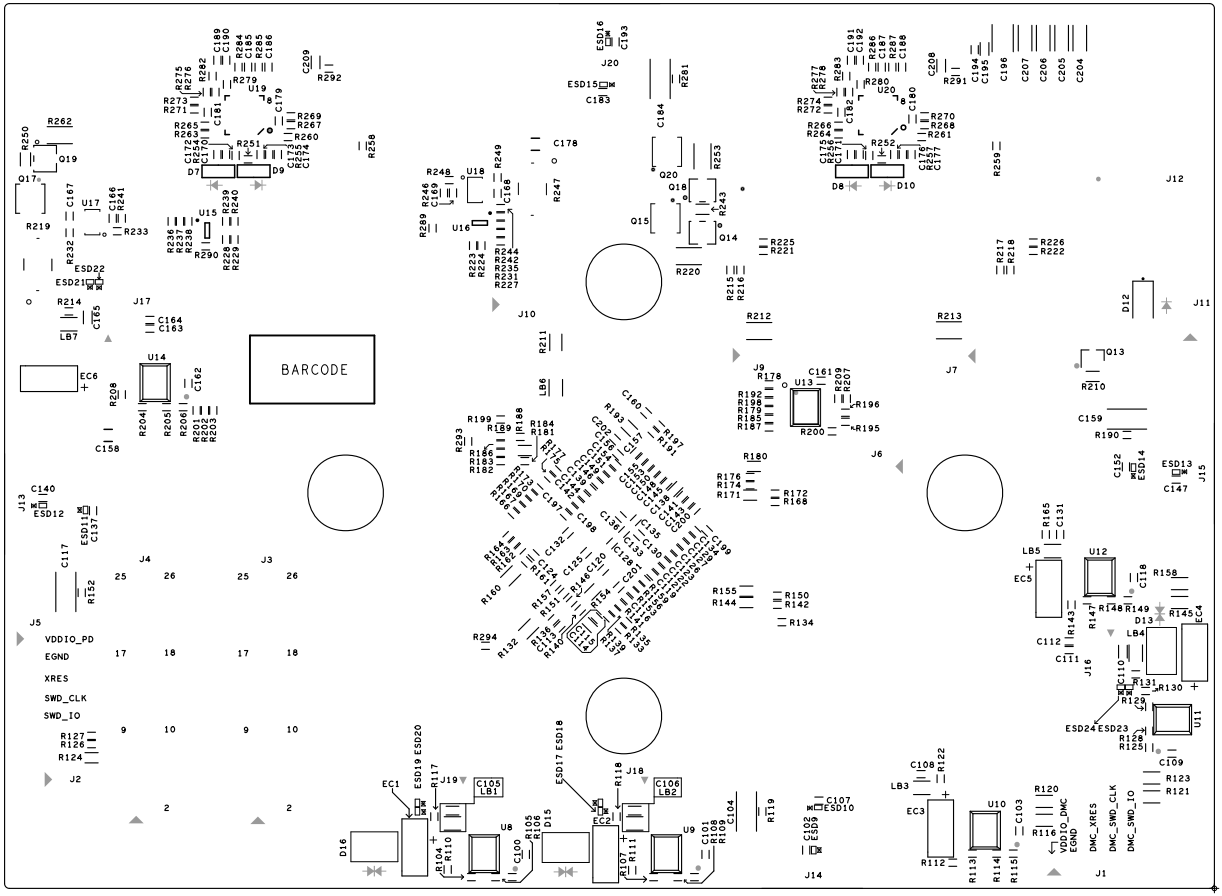
	DRAWN BY: HUSA		
	LAYER: SECONDARY SIDE SOLDERPASTE		
SAN JOSE, CA 95134 (408) 943-2600	DWG NO: 600-60512-01	REV: 03	DATE: 13/12/18



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SAN JOSE, CA 95134 (408) 943-2600	DRAWN BY: HUSA		
	LAYER: SECONDARY SIDE SILKSCREEN		
	DWG NO: 600-60512-01	REV: 03	DATE: 13/12/18